# AND8373/D

# 2 Switch-Forward Current Mode Converter

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**APPLICATION NOTE**

### Introduction

A major advantage of the two−switch forward converter is that the power switches only block the supply voltage instead of twice the supply voltage as in the flyback or single−switch forward converter.

Here after, the complete specification, of the two switch−forward converter is described:

**Table 1. Specification**

| Description | Value | Units |
|---|---|---|
| Input voltage Range | 350−410 | Vdc |
| Output Voltage | 12 | Vdc |
| Output Power | 96 | W |
| Output Peak Power during 5 sec per 1 min | 120 | W |
| Minimum Output Load Current(s) | 0 | Adc |
| Number of Outputs | 1 | |
| Nominal Output Voltage | 12 ±5% | Vdc |
| Maximum Output Current | 8 | Adc |
| Maximum Output Peak Current | 10 | Adc |
| Output ripple | 50 | mV |
| Maximum startup time | < 1 | s |
| Standby Power | < 100 | mW |
| Target Efficiency at full load @ Vin = 390 V dc | 90 | % |
| Load Conditions for Efficiency Measurements (10%, 20%,..) | 20, 50 & 100 | % |
| Min Load Efficiency (Pout = 1.2 W) | > 50 | % |
| Maximum Transient load step of the maximum output current | 50 | % |
| Maximum Output drop voltage from $I_{out}$ = 5 to 10 A in 5 μs | 250 | mV |

This application note describes the design of 120−W, 125 kHz, two−switch forward current mode converter with the NCP1252 controller. It can viewed the practical implementation of the 2−switch forward converter example described in Ref. [1].

The NCP1252 controller offers everything to build cost−effective and reliable ac−dc switching power supplies implementing the forward converter: NCP1252 detects an output overload without relying on the auxiliary Vcc, a Brown−Out input offers protection against low input voltages and improves the converter safety. Finally a SOIC8 package saves PCB space and represents a solution of choice in cost sensitive projects.

The power supply described here operates from a dc input voltage, as the forward converter is usually connected after a Power Factor Correction (PFC) stage. It generates a 12−V output at 10 A. The efficiency at full load is close to 90% at the nominal output of the PFC.

## Power Supply Components Calculation

### Transformer

The following equation extracted from the buck converter running in Continuous Current Mode (CCM), turns ratio will determine the turns ratio of the transformer:

$$V_{out} = \eta \cdot V_{bulk\ min} \cdot DC_{max} \cdot N \qquad \text{(eq. 1)}$$

Where:

- $V_{out}$ is the output voltage
- $\eta$ is the targeted efficiency
- $V_{bulkmin}$ is the minimum operating input voltage of the forward
- $DC_{max}$ is the maximum duty cycle that the NCP1252 can deliver
- N is the turns ratio of the transformer

Extracting the turns ratio from the previous equation, we obtain:

$$N = \frac{V_{out}}{\eta V_{bulk\ min} DC_{max}} = \frac{12}{0.9 \times 350 \times 0.45} = 0.085 \qquad \text{(eq. 2)}$$

Using this value in Equation 1, we can estimate the minimum duty cycle at high line by changing the bulk voltage parameter:

$$DC_{min} = \frac{V_{out}}{\eta V_{bulk\ max} N} = \frac{12}{0.9 \times 410 \times 0.085} = 38.2\% \quad \text{(eq. 3)}$$

To ensure enough primary magnetizing current to properly reset the core (drive the stray capacitance and allow the voltage across the winding to reverse), one must usually reduce the primary inductance from the core's ungapped value to one that will cause an adequate magnetizing current. A popular rule of thumb as to make the magnetizing current around 10% of the primary current. Since the primary current is 0.94 A peak (the calculation of this peak current is given on the following paragraph), we will let the magnetizing current rise to 0.1 A. The desired primary inductance, then, with a primary voltage of 350 Vdc and a pulse duration of 3.6 μs

$$\left(\frac{DC_{max}}{F_{sw}} = \frac{0.45}{125\ k}\right), \text{ is}$$

$$L_{mag} = \frac{V_{bulkmin}}{\frac{10\%I_{p\_pk}}{\frac{DC_{max}}{F_{sw}}}} = \frac{350}{\frac{0.1 \times 0.94}{\frac{0.45}{125\ k}}} = 13.4\ mH \quad \text{(eq. 4)}$$

Based on this assumption the transformer manufacturer offered the following transformer core: E30/15/7.

**LC Output Filter:**

The crossover frequency $f_c$ will arbitrarily be selected at 10 kHz. Beyond this value, the converter would pick−up switching noise and would require a more carefull layout. Below, the stringent dropout specification would lead to the selection of a larger output capacitor. Considering a voltage drop mostly dictated by $f_c$, the output capacitance and the step load current, we can derive a first capacitor value by using a formula already encountered:

$$C_{out} \geq \frac{\Delta I_{out}}{2\pi f_c \Delta V_{out}} \geq \frac{5}{2\pi \times 10\ k \times 0.25} \geq 318\ \mu F \quad \text{(eq. 5)}$$

The above case assumes an ESR much lower than the capacitor impedance at the crossover frequency:

$$R_{ESR} \leq \frac{1}{2\pi f_c C_{out}} \leq \frac{1}{2\pi \times 10\ k \times 318\ \mu} \leq 50\ m\Omega \quad \text{(eq. 6)}$$

We must also select a capacitor whose worst case ESR remains below the capacitor impedance at the crossover frequency, in order to limits its contribution to the transient output drop. We are going to parallel two 1000 μF FM capacitors from Panasonic.

C = 2000 μF, FM series @ 16 V

$I_{C,rms}$ = 5.36 A (2*2.38 A) @ $T_A$ = +105°C

$R_{ESR,low}$ = 8.5 mΩ (19 mΩ/2) @ $T_A$ = +20°C

$R_{ESR,high}$ = 28.5 mΩ (57 mΩ/2) @ $T_A$ = −10°C

Given a $\Delta I_{out}$ of 5 A, the above room temperature ESR components would, generate an output voltage undershoot/overshoot of:

$$\Delta V_{out} = \Delta I_{out} R_{ESR,max} = 5 \times 28.5\ m = 142\ mV \quad \text{(eq. 7)}$$

which is acceptable given a specification of 250 mV.

There is a rule of thumb to select an ESR capacitor equal to the half of the calculated value with Equation 6. This rule will take into account the process variation of the capacitor plus some margin for a startup operation of the power supply at very low ambient temperature.

The final check will include the circulating rms current. However, given the nonpulsating nature of the buck output, we do not expect this current to be that high.

Considering the output power level and the selected capacitor, we can consider the total ripple voltage contributed by the ESR term alone. Thus, if we adopt an ESR of 22 mΩ (approximate value at 0°C), the maximum peak to peak output ripple current must be lower than:

$$\Delta I_L \leq \frac{V_{ripple}}{R_{ESR,max}} \leq \frac{50\ m}{22\ m} \leq 2.27\ A \quad \text{(eq. 8)}$$

To obtain the output inductor value, we can write the buck ripple expression based on the off−time duration:

$$\Delta I_L = \frac{V_{out}}{L}(1 - DC_{min})T_{sw} \quad \text{(eq. 9)}$$

Using Equation 8, we can derive a minimum inductor value for L:

$$L = \frac{V_{out}}{\Delta I_L}(1 - DC_{min})T_{sw} \geq \frac{12}{2.27}(1 - 0.38)\frac{1}{125\ k} \geq 26\ \mu H \quad \text{(eq. 10)}$$

If we consider a 10% drop in the inductor value at high temperature and current, let us adopt a 29 μH output inductor. But as this value is not standard part we will stick to a 27−μH normalized value.

With the selected inductor value, we can calculate the rms current in the output capacitor:

$$I_{C_{out},rms} = I_{out}\frac{1 - DC_{min}}{\sqrt{12\tau_L}} = 10 \times \frac{1 - 0.38}{\sqrt{12 \times 2.813}} = 1.06\ A \quad \text{(eq. 11)}$$

Where:

$$\tau_L = \frac{L_{out}}{\frac{V_{out}}{I_{out}} \cdot \frac{1}{F_{sw}}} = \frac{27\ \mu}{\frac{12}{10} \times \frac{1}{125\ k}} = 2.813 \quad \text{(eq. 12)}$$

Given the equivalent capacitor current capability (5.36 A), there is no problem here.

The secondary side peak current will be:

$$I_{s\_pk} = I_{out} + \frac{\Delta I_L}{2} = 10 + \frac{2.27}{2} = 11.13\ A \quad \text{(eq. 13)}$$

On the primary side, this current reflects to:

$$I_{p\_pk} = I_{s\_pk} N_{ratio} = 11.13 \times 0.085 = 0.946\ A \quad \text{(eq. 14)}$$

And the valley reaches

$$I_{p\_valley} = \left(I_{out} - \frac{\Delta I_L}{2}\right)N_{ratio} = \left(10 - \frac{2.27}{2}\right) \times 0.085 = 0.75\ A \quad \text{(eq. 15)}$$

Based on the following Equation 16, we are able to calculate the rms current of a pulsating waveform with linear current (see Figure 1):

$$I_{rms} = I\sqrt{DC}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta I}{2I}\right)} \quad \text{(eq. 16)}$$

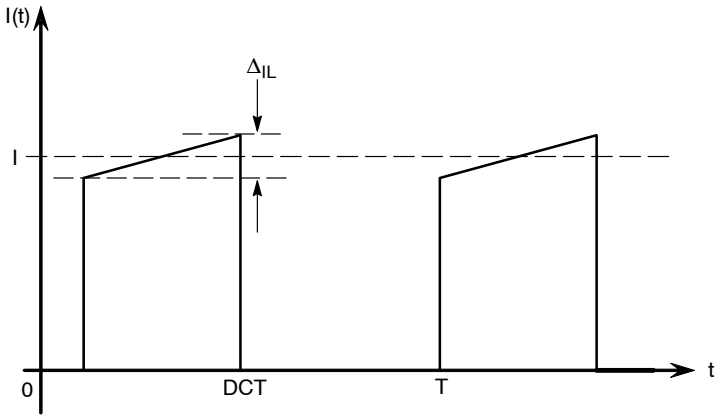


**Figure 1. Pulsating Waveform with Linear Ripple Current**

This waveform exactly despits the current we have with a forward converter on the primary or secondary side of the tranformer.

When this current is measured on the primary side, ΔI represents the reflected secondary−side ripple summed with the magnetizing current. Thus if we would like to accurately calculate the primary rms current, the magnetizing current should be added to the $I_{p\_pk}$ calculated with Equation 14. The magnetizing inductance has been previously calculated (Equation 4) with 10% of the primary peak current. Therefore the primary rms current can be written has followed:

$$I_{p,rms,10\%} = \sqrt{DC_{max}\left((1.1 \cdot I_{p\_pk})^2 - 1.1 \cdot I_{p\_pk}\Delta I_L N + \frac{(\Delta I_L N)^2}{3}\right)} \quad \text{(eq. 17)}$$

$$I_{p,rms,10\%} = \sqrt{0.45\left((1.1 \times 0.946)^2 - 1.1 \times 0.946 \times 2.27 \times 0.085 + \frac{(2.27 \times 0.085)^2}{3}\right)} = 0.63\ A$$

Where:

- $DC_{max}$ is the maximum duty cycle that the NCP1252 can deliver
- $I_{p\_pk}$ is the peak current calculated by Equation 14.
- $\Delta I_L$ is the maximum output peak to peak current ripple
- N is the turns ratio of the transformer

### Mosfet Selection

The mosfets are selected based on the maximum input voltage and a derating factor $k_M$ of 0.85. If we choose 500 V devices (in a two−switch forward converter, the transistor stress is limited to the input voltage), the maximum high−voltage rail must be limited to

$$V_{bulk,max} = BV_{DSS}k_M = 500 \times 0.85 = 425\ V \quad \text{(eq. 18)}$$

If the PFC does not include skip cycle in light−load operation, chances are that its output voltage will reach the overvoltage protection (OVP) level. The converter thus enters a kind of autorecovery hiccup mode. It is therefore important to check that one respects Equation 18 despite the OVP detection.

The FDP16N50 has been selected for this application. Its specification are as follows:

- Package TO220
- $BV_{DSS}$ = 500 V
- $R_{DS(on)}$ = 0.434 Ω at $T_j$ = 110°C ($R_{DS(on)}$ = 0.31 Ω @ $T_j$ = 25°C multiplied by 1.4: $R_{DS(on)}$ derating factor for 110°C)
- $Q_G$ = 45 nC
- $Q_{GD}$ = 14 nC

Thanks to Equation 17, we can estimate its conduction losses as

$$P_{cond} = I_{p,rms,10\%}{}^2\, R_{DS(on)} @\ T_J = 110°C = 0.632^2 \times 0.434 = 173\ mW \quad \text{(eq. 19)}$$

As we are running a 2−switch forward application, the voltage presents on each power switch at the turn−on is equal to the half of the bulk voltage: the two following figures illustrate the 2−switch forward arrangement and the simulated voltage present on both power switches.

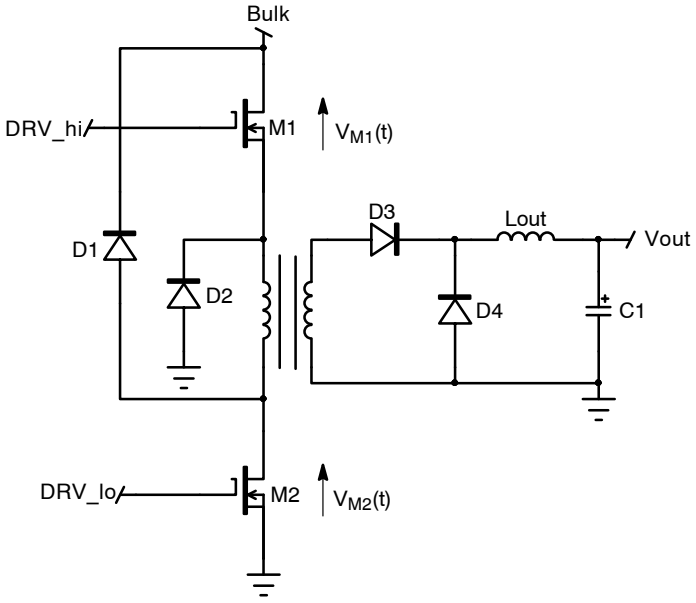


**Figure 2. 2−switch Forward Arrangement**

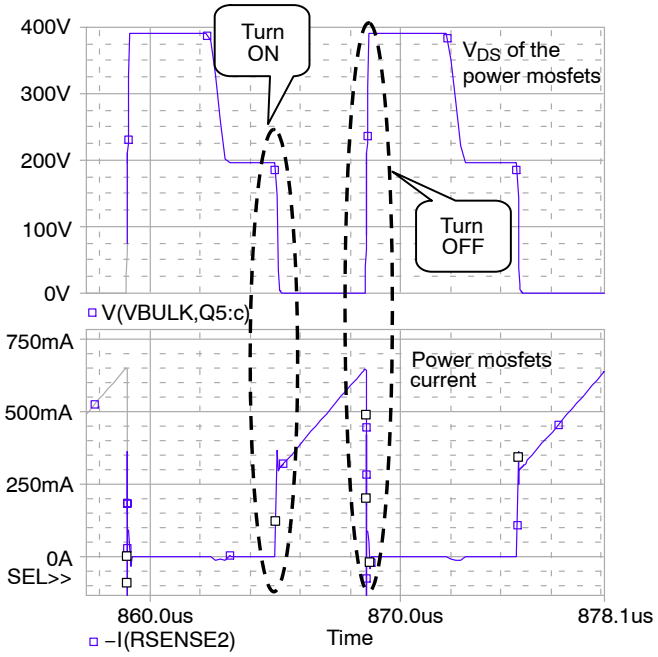


**Figure 3. Power Mosfet Curves: $V_{DS}(t)$ and $I_D(t)$ of the Both Power Mosfets**

At the turn−on the power losses can be expressed as follow:

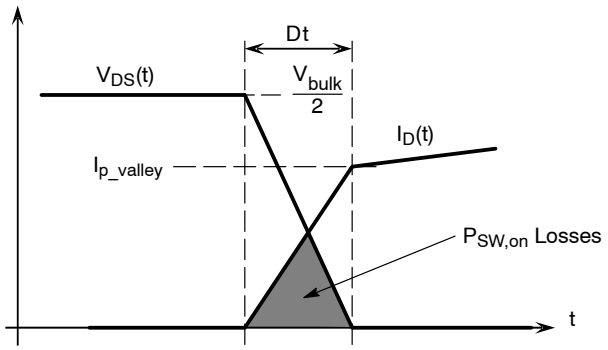


**Figure 4. Turn−on Losses ($P_{SW,on}$)**

The average power losses at the switch on is a triangle area, the exact calculation can be done via the following integral calculation:

$$P_{SW,on} = F_{sw}\int_0^{\Delta t} I_D(t)V_{DS}(t)dt = \frac{I_{p\_valley}\frac{V_{bulk}}{2}\Delta t}{6}F_{sw} \quad \text{(eq. 20)}$$

$$P_{SW,on} = \frac{I_{p\_valley}V_{bulk}\Delta t}{12}F_{sw}$$

Based on the previous equation we are able to estimate the losses at each power mosfet switch on:

$$P_{SW,on} = \frac{I_{p\_valley}V_{bulk,max}\Delta t}{12}F_{sw} \quad \text{(eq. 21)}$$

$$P_{SW,on} = \frac{0.75 \times 410 \times 46.7\ n}{12} \times 125\ k = 149\ mW$$

Where the overlap (Δt) is estimated via the following equation:

$$\Delta t = \frac{Q_{GD}}{I_{DRV\_pk}} = \frac{14\ n}{0.300} = 46.7\ ns \quad \text{(eq. 22)}$$

This overlap estimation does not take into account that the driver of the NCP1252 is a CMOS type, in that case the output driver will not deliver a constant current. Nevertheless the estimation is not so wrong. This overlap is true for a bipolar driver stage that it delivers a constant current.

As we have 2 power mosfets with our application the total switch−on losses will the double of the losses from Equation 21: 358 mW.

Experimental measurement:

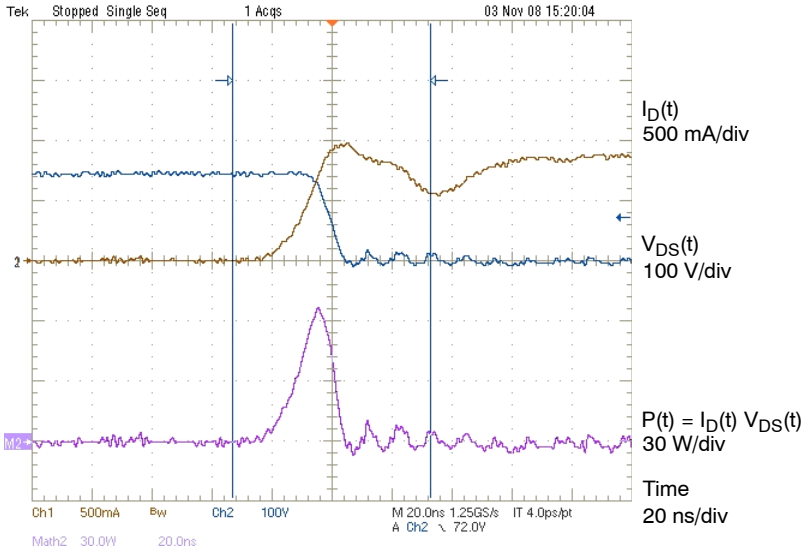


**Figure 5. Switching Losses During the Turn On of the LOW Side Mosfet**

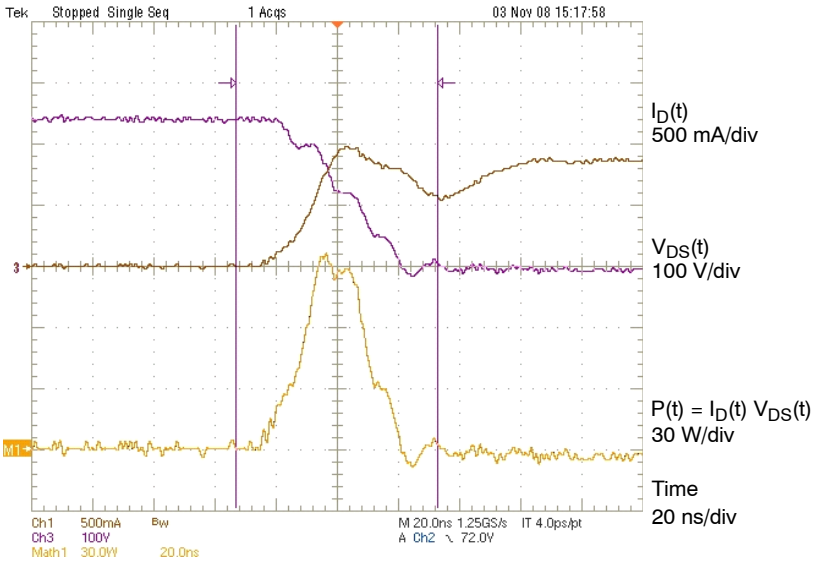


**Figure 6. Switching losses during the turn on of the HIGH side mosfet**

Figures 5 and 6 represent the power losses of the power mosfets (high and low side mosfet). From these figures we can note that the drain to source voltage on the low and high side mosfet is not at the half of bulk voltage as expected from the theory and the simulation result.

Drain to source power mosfet voltage is not equal to the half of the bulk voltage due to the parasitic element from the transformer and the power mosfet. The low side power mosfet voltage is equal to 150 V and 240 V for the high side one.

Thus the measured switch−on losses are the following:

- High side switch on losses: 386 mW
- Low side switch on losses: 155 mW

If we compare these experimental results with the theory from Equation 21 where the switch on losses has been estimated to 179 mW per switch, we can conclude that the losses have not been well estimated. This is probably due to the wrong estimation of the driver current capability ($I_{DRV\_pk}$): we took the hypothesis that the driver is able to deliver a constant current as we have with a bipolar output stage (UC384X like). But as the NCP1252's output driver stage is based on the CMOS technology, the current is varying with the voltage on the power mosfet gate, thus it is really difficult to estimate accurately the overlap.

As the losses of the power MOSFET in a 2−switch forward are very low, the error introduce in these estimations does not impact to much the heat sink calculation.

The losses at the turn off can be calculated using the similar method: but now the peak current is at its max value. The drain−to−source voltage of the power switch is close to zero and switches to $V_{bulk}$.

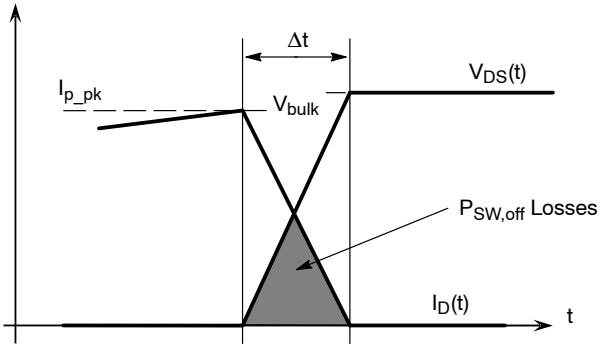


**Figure 7. Turn−off Losses ($P_{SW,off}$)**

Based on the equation used for the switch on losses, we are able to estimate the losses at each power mosfet:

$$P_{SW,off} = \frac{I_{p\_pk} V_{bulk,max} \Delta t}{6} F_{sw} = \frac{0.95 \times 410 \times 40\ n}{6} \times 125\ k = 324\ mW \quad \text{(eq. 23)}$$

The overlap (Δt) is estimated via the following equation:

$$\Delta t = \frac{Q_{GD}}{I_{DRV\_pk}} = \frac{14\ n}{0.350} = 40\ ns \quad \text{(eq. 24)}$$

We are now able to estimate the overall losses on each power mosfet:

$$P_{losses} = P_{SW,on} + P_{cond} + P_{SW,off} = 0.149 + 0.173 + 0.324 \quad \text{(eq. 25)}$$
$$P_{losses} = 646\ mW$$

Where:

- Switch−on losses: $P_{SW,on}$ = 149 mW
- Conduction losses: $P_{cond}$ = 173 mW
- Switch−off losses: $P_{SW,off}$ = 324 mW

Once we have the total dissipation budget per MOSFET, a heatsink can be calculated.

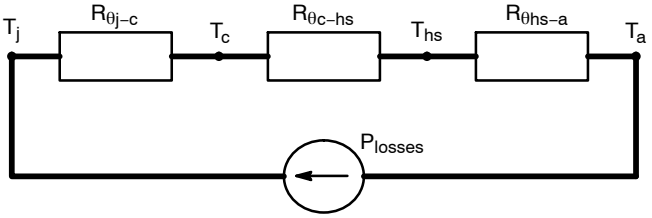


**Figure 8. Thermal path between the power mosfet and the heat sink**

Where:

- $T_j$ is the junction temperature of the power mosfet
- $T_c$ is the case temperature of the power mosfet
- $T_{hs}$ is the heat sink temperature
- $T_a$ is the ambient temperature
- $R_{\theta j-c}$ is the thermal resistance between the junction and the case of the power mosfet
- $R_{\theta c-hs}$ is the thermal resistance between the case of the power mosfet and the heat sink
- $R_{\theta hs-a}$ is the thermal resistance between the heat sink and the ambient temperature.

The following condition has to be checked to prevent any over heating of the power mosfet during worst case operation:

$$T_{jmax} - T_{ambmax} > P_{losses} \sum R_{\theta} \quad \text{(eq. 26)}$$

Or it can be written as follow:

$$R_{\theta hsa} < \frac{T_{jmax} - T_{ambmax}}{P_{losses}} - \left(R_{\theta jc} + R_{\theta chs}\right) < \frac{110 - 65}{0.646} - (1 + 1.2) \quad \text{(eq. 27)}$$
$$R_{\theta hsa} < 67.4°C/W$$

Thus the thermal resistance of the heat sink should be lower than 67.4°C/W. A KL194/25.4/SW from Seifert (ref.[2]) has been selected (14°C/W).

### Diodes Selection

The choice of the primary freewheeling diodes depends on the transformer magnetizing inductor. The magnetizing peak current can be calculated via the following equation:

$$I_{mag\_pk} = \frac{V_{bulk,min}}{L_{mag}} \frac{DC_{max}}{F_{sw}} = \frac{350}{13.4\ m} \times \frac{45\%}{125\ k} = 94\ mA \quad \text{(eq. 28)}$$

As the magnetizing and demagnetizing voltage are similar ($V_{bulk}$, thanks to the 2−switch forward structure); both on and reset times are equal.

$$t_{reset} = I_{mag,pk} \frac{L_{mag}}{V_{bulkmin}} = 94\ m \frac{13.4\ m}{350} = 3.6\ \mu s \quad \text{(eq. 29)}$$

The average current can now be derived in a snapshot:

$$I_{mag\_avg} = \frac{(t_{on} + t_{reset}) I_{mag\_pk}}{\frac{2}{F_{sw}}} = \frac{\left(\frac{DC_{max}}{F_{sw}} + t_{reset}\right) I_{mag\_pk}}{\frac{2}{F_{sw}}} = \frac{\left(\frac{0.45}{125\ k} + 3.6\ \mu\right) \times 94\ m}{\frac{2}{125\ k}} \quad \text{(eq. 30)}$$
$$I_{mag\_avg} = 42.3\ mA$$

Diode such as the MUR160 accommodates the demagnetization task easily. Usually, in off−line application as the magnetizing current remains low any 1 A high voltage diode (500 or 600 V) can do the job.

Let us now take care of the secondary diodes. In the forward converter, both secondary−side diodes sustain a similar peak inverse voltage (PIV). Given a turns ratio of 0.085 and the diode's derating factor $k_D$, the diodes have to sustain the following PIV:

$$PIV = \frac{N V_{bulkmax}}{k_D} = \frac{0.085 \times 410}{0.60} = 58\ V \quad \text{(eq. 31)}$$

Thanks to the low PIV value, we are able to select the following Schottky diode reference: MBRB30H60CT.

This diode (30 A, 60 V in a TO−220) case features a maximum drop of 0.5 V at 125°C (see Figure 9)

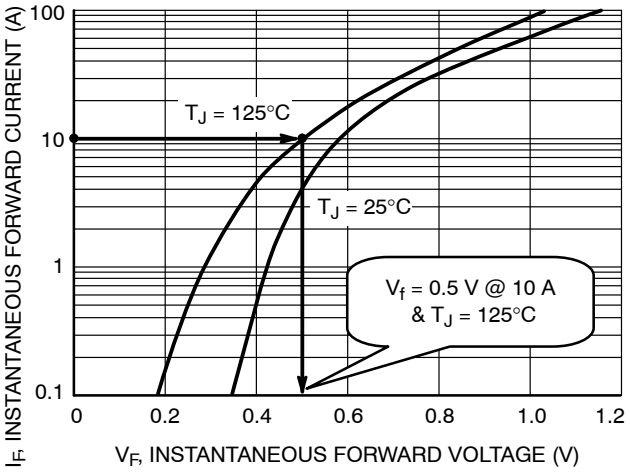


**Figure 9. MBRB30H60CT, Maximum Forward Voltage versus Instaneous Current**

The series diode would then dissipate the following power in worst case conditions (Low line and maximum duty cycle).

$$P_{d\_on} = V_f I_{out} DC_{max} = 0.5 \times 10 \times 0.45 = 2.25\ W \quad \text{(eq. 32)}$$

The freewheeling diode would dissipate slightly more as it conducts during the off time:

$$P_{d\_off} = V_f I_{out}(1 - DC_{min}) = 0.5 \times 10 \times (1 - 0.39) = 3.05\ W \quad \text{(eq. 33)}$$

On average these diodes would dissipate around 5.3 W or 4.4% of the total output power. In order to improve the efficiency it can be interesting to implement a synchronous rectification to replace them.

For these diodes, we can re−use Equation 27 to calculate the required heat sink.

$$R_{\theta hs-a} < \frac{T_{Jmax} - T_{AMBmax}}{P_{losses}} - \left(R_{\theta j-c} + R_{\theta c-hs}\right) < \frac{125 - 65}{5.33} - (2 + 1.2) \quad \text{(eq. 34)}$$

$$R_{\theta hs-a} < 8.06°C/W$$

Thus the thermal resistance of the heat sink should be lower than 8°C/W.

For the demonstration board, the following heat sink has been selected KL195/25.4/SW from Seifert (ref.[2]). It provides a low thermal resistance of 6.2°C/W.

## NCP1252 Component Selection

### Switching Frequency Selection

A resistor connected between the $R_t$ pin and the ground precisely sets the switching frequency between 50 kHz and a maximum of 500 kHz. The following curve helps to select the resistor according the selected switching frequency.

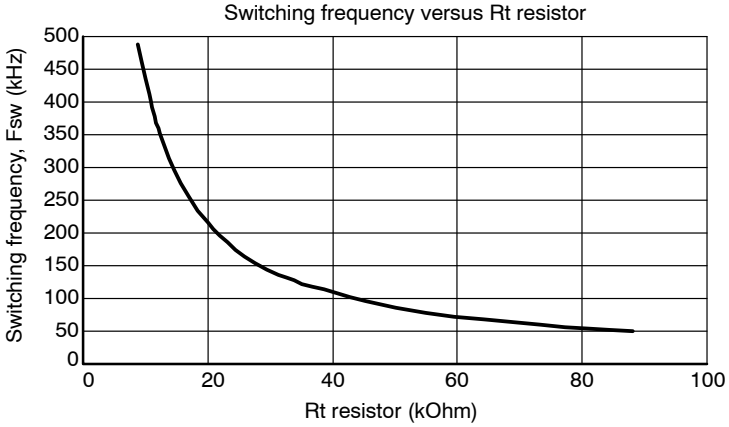


**Figure 10. Switching Frequency Selection**

The following equation could also be used to calculate the resistor value according to the switching frequency selection:

$$R_t = \frac{1.95 \times 10^9 V_{R_t}}{F_{sw}} \quad \text{(eq. 35)}$$

Where:

- $V_{Rt}$ is the internal voltage reference present on the Rt pin and equal to 2.2 V.

If we assume a switching frequency of 125 kHz,

$$R_t = \frac{1.95 \times 10^9 \times 2.2}{125\ k} = 34.3\ k\Omega$$

If we select a 33 kΩ resistor, this will yield:

$$F_{sw} = \frac{1.95 \times 10^9 V_{R_t}}{R_t} = \frac{1.95 \times 10^9 \times 2.2}{33\ k} = 130\ kHz \quad \text{(eq. 36)}$$

The measurement on the final board with a resistor equal to 33 kΩ gives us 130 kHz for the switching frequency.

This oscillator resistor will be laid out as close as possible to the Rt pin (pin #4) of the NCP1252 and its ground (pin #5). As these pins are really close together, it will be not so difficult to take into account this requirement. The robustness of the controller against electrical noise will be improved.

### Sense Resistor

The NCP1252 featuring a maximum peak current to 1 V, the sense resistor is computed via the following expression, where a 20% margin appears on the primary peak current (10% for the magnetizing current and 10% for general margin):

$$R_{sense} = \frac{F_{CS}}{1.2 I_{p\_pk}} = \frac{1}{1.2 \times 0.946} = 884\ m\Omega \quad \text{(eq. 37)}$$

The power dissipation of the sense resistor with a 20% margin on the primary peak current amounts to:

$$P_{R_{sense}} = I_{p,rms,20\%}{}^2 R_{sense} = 0.695^2 \times 0.884 = 427\ mW \quad \text{(eq. 38)}$$

Where:

- $I_{p,rms,20\%}$ is the rms current of the primary peak current with 20% margin on the peak current

As we are using 1206 resistor type sizes with a limited power dissipation of 250 mW, we have to place 2 resistors in parallel in order to fit the authorized power capability. Thus we select 2 resistors of 1.5 Ω. The new power dissipation will be 362 mW for both resistors and 180 mW for each one.

Despite the presence of a Leading Edge Blanking (LEB = 130 ns), it is recommended to insert between the sense resistor and the CS pin of the controller a small RC filter in order to remove any parasitic noise from the application. This small RC network will "clean" the current sense measurement and it will improve the robustness of the power supply. Nevertheless this time constant should not be too large compared to the switching period of the controller. It is usually recommended to select a 150−300−ns time constant for the current sense filter network.

The NCP1252 provides an internal ramp compensation appearing on the CS pin. The resistor of the RC filter will play a double function: ramp compensation and time constant for filtering. Thus the ramp compensation will fix the resistor value of the RC filter and then the capacitor will be adjusted to respect the time constant previously defined.

One of the following chapters describes how to calculate the ramp compensation resistor.

### Brown−out

By monitoring the level on BO pin, the NCP1252 protects the forward converter against low input voltage conditions. When the BO pin level falls below the $V_{BO}$ level, the controllers stops pulsing until the input level goes back to normal and resumes the operation via a new soft start sequence.

The brown−out comparator features a fixed voltage reference level ($V_{BO}$). The hysteresis is implemented by using the internal current connected between the BO pin and the ground when the BO pin is below the internal voltage reference ($V_{BO}$).

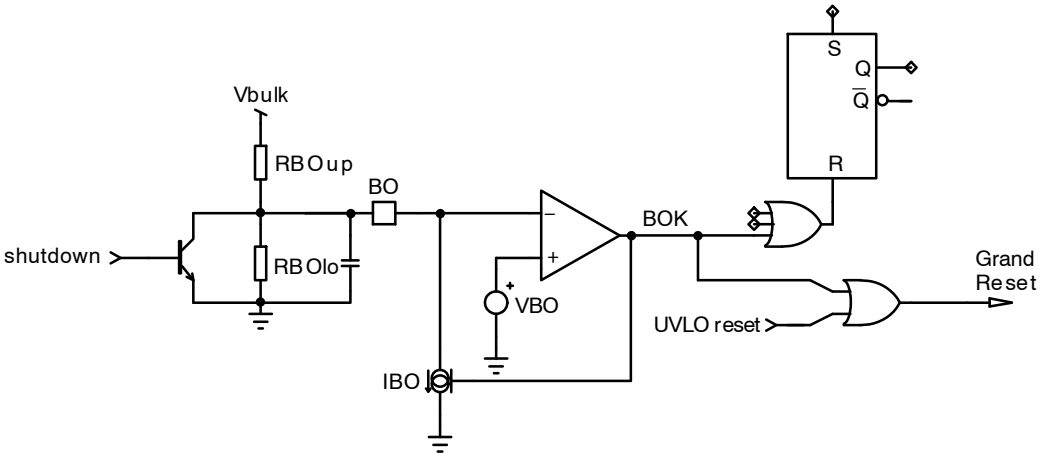


**Figure 11. BO Pin Setup**

The following equations show how to calculate the resistors for BO pin.

First of all, select the bulk voltage value at which the controller must start switching ($V_{bulkon}$) and the bulk voltage for shutdown ($V_{bulkoff}$) the controller.

Where:

- $V_{bulkon}$ = 370 V
- $V_{bulkoff}$ = 350 V
- $V_{BO}$ = 1 V (fixed internal voltage reference)
- $I_{BO}$ = 10 μA (fixed internal current source)

When BO pin voltage is below $V_{BO}$ (internal voltage reference), the internal current source ($I_{BO}$) is activated. The following equation can be written:

$$V_{bulkON} = R_{BOup}\left(I_{BO} + \frac{V_{BO}}{R_{BOlo}}\right) + V_{BO} \quad \text{(eq. 39)}$$

When BO pin voltage is higher than $V_{BO}$, the internal current source is now disabled. The following equation can be written:

$$V_{BO} = \frac{V_{bulkoff} R_{BOlo}}{R_{BOlo} + R_{BOup}} \quad \text{(eq. 40)}$$

From Equation 40 $R_{BOup}$ can be extracted:

$$R_{BOup} = \left(\frac{V_{bulkoff} - V_{BO}}{V_{BO}}\right)R_{BOlo} \quad \text{(eq. 41)}$$

Equation 41 is substituted in Equation 39 and solved for $R_{BOlo}$, yields:

$$R_{BOlo} = \frac{V_{BO}}{I_{BO}}\left(\frac{V_{bulkon} - V_{BO}}{V_{bulkoff} - V_{BO}} - 1\right) \quad \text{(eq. 42)}$$

$R_{BOup}$ can be also written independently of $R_{BOlo}$ by substituting Equation 42 into Equation 41 as follow:

$$R_{BOup} = \frac{V_{bulkon} - V_{bulkoff}}{I_{BO}} \quad \text{(eq. 43)}$$

From Equation 42 and Equation 43, the resistor divider value can be calculated:

$$R_{BOlo} = \frac{1}{10\,\mu}\left(\frac{370 - 1}{350 - 1} - 1\right) = 5731\ \Omega$$

$$R_{BOup} = \frac{370 - 350}{10\,\mu} = 2.0\ M\Omega$$

We selected the following values for the brown out resistor divider:

- $R_{BOlo}$ = 5.1 KΩ + 680 Ω
- $R_{BOup}$ = 1 MΩ + 1 MΩ

### Soft Start

The soft start of the NCP1252 controls the peak current of the forward converter during the startup sequence: this prevent any over stress on the power components (primary mosfet, secondary diode and magnetic component like transformer and inductor) during this critical phase and it reduces the output overshoot.

The soft start pin provides a current source connected to an internal voltage reference. Thus a capacitor connected to this current source generates a linear voltage slope that controlling the peak current of the power supply via the current sense resistor. The SS pin voltage is divided by 4 to scale down the SS pin voltage to a compatible CS pin voltage.

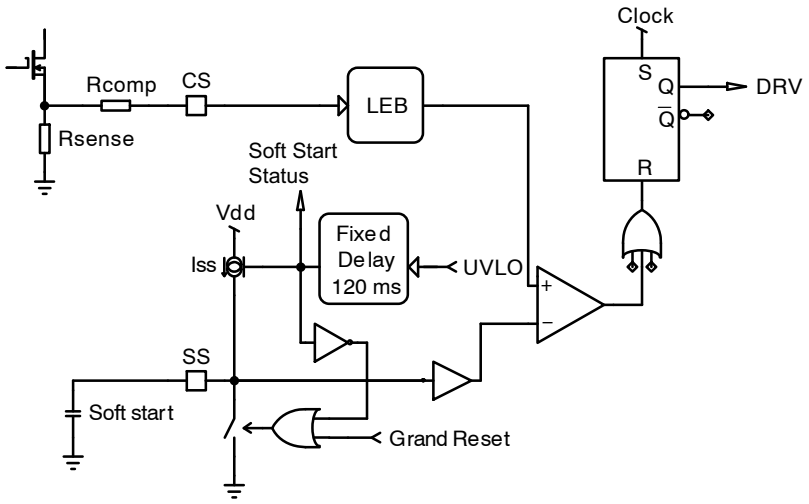


**Figure 12. Soft Start Principle**

Based on the following well known equation:

$$I_{SS} = C_{SS}\frac{V_{SS}}{T_{SS}} \quad \text{(eq. 44)}$$

By extracting from the previous equation the capacitor value we are able to calculate the soft start duration: if we select $T_{ss}$ = 15 ms,

$$C_{SS} = I_{SS}\frac{T_{SS}}{V_{SS}} = 10\,\mu\frac{15\ m}{4.0} = 37.5\ nF \quad \text{(eq. 45)}$$

If we select $C_{ss}$ = 33 nF, the soft start duration measured (see Figure 13) on the demoboard is equal to 13 ms.

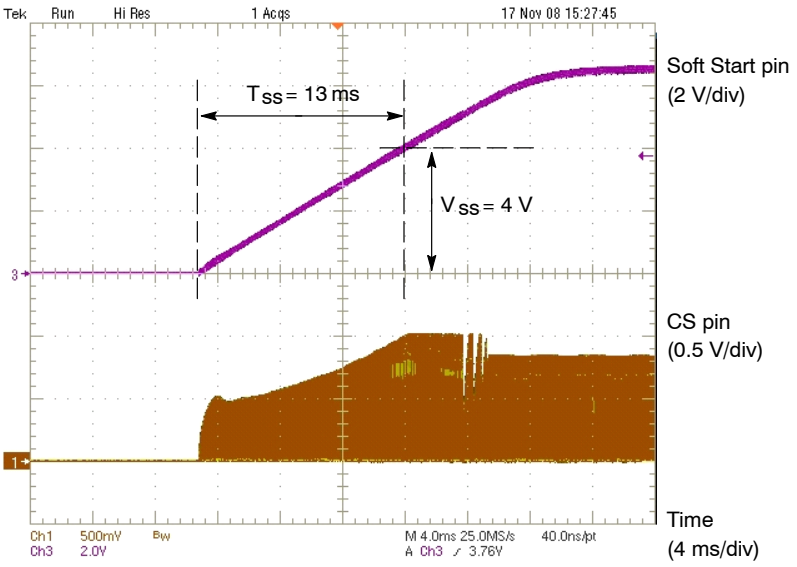


**Figure 13. Soft Start Duration Illustration**

Figure 13 illustrates that the max voltage on the soft start pin is equal to 6.6 V, but the peak current of the forward transformer linearly ramps from zero to 4.0 V. Above 4.0 V on the SS pin, the controller will clamp to the max peak current.

At the beginning of the soft start the peak current variation is not linear due to the Discontinuous Mode Current (DCM) operation of the forward at low peak current and low voltage on the output.

### Ramp Compensation Selection

Ramp compensation is a known means to cure subharmonic oscillations. These oscillations take place at half of the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−cycle close or above 50%. To lower the current loop gain, one usually injects between 50 and 100% of the inductor downslope. Figure 14 depicts how internally the ramp is generated:

The ramp compensation applied on CS pin is buffered from the internal oscillator ramp. A switch placed between the buffered internal oscillator ramp and $R_{ramp}$ disconnects the ramp compensation during the off−time DRV signal.

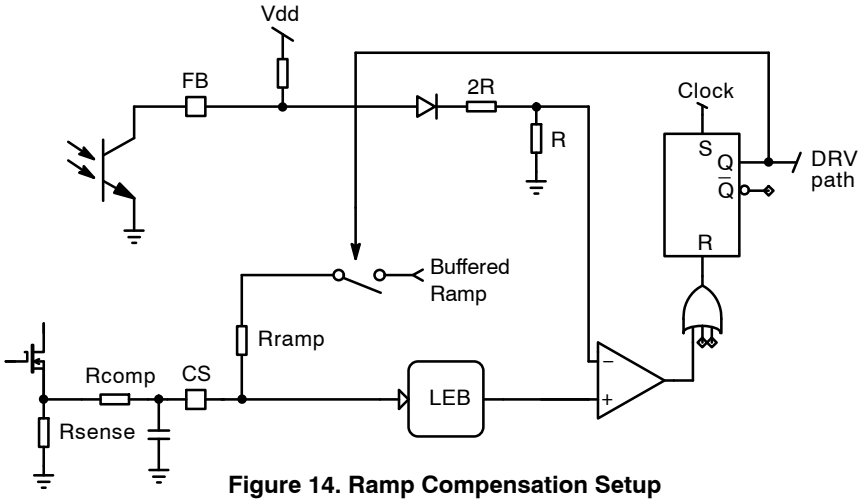


**Figure 14. Ramp Compensation Setup**

In the NCP1252, the internal ramp swings with a slope of:

$$S_{int} = \frac{V_{ramp}}{DC_{max}} F_{sw} \qquad \text{(eq. 46)}$$

In a forward application the secondary−side downslope viewed on a primary side requires a projection over the sense resistor $R_{sense}$. Thus:

$$S_{sense} = \frac{(V_{out} + V_f)}{L_{out}} \frac{N_S}{N_P} R_{sense} \qquad \text{(eq. 47)}$$

where:

- $V_{out}$ is output voltage level
- $V_f$ the freewheel diode forward drop
- $L_{out}$, the secondary inductor value
- $N_s/N_p$ the transformer turn ratio
- $R_{sense}$: the sense resistor on the primary side

Assuming the selected amount of ramp compensation to be applied is $\delta_{comp}$, then we must calculate the division ratio to scale down $S_{int}$ accordingly:

$$\text{Ratio} = \frac{S_{sense}\delta_{comp}}{S_{int}} \quad \text{(eq. 48)}$$

A few line of algebra determined $R_{comp}$:

$$R_{comp} = R_{ramp}\frac{\text{Ratio}}{1 - \text{Ratio}} \quad \text{(eq. 49)}$$

The previous ramp compensation calculation does not take into account the natural primary ramp created by the transformer magnetizing inductance. In some case illustrate here after the power supply does not need additional ramp compensation due to the high level of the natural primary ramp.

The natural primary ramp is extracted from the following formula:

$$S_{natural} = \frac{V_{bulk}}{L_{mag}}R_{sense} \quad \text{(eq. 50)}$$

Then the natural ramp compensation will be:

$$\delta_{natural\_comp} = \frac{S_{natural}}{S_{sense}} \quad \text{(eq. 51)}$$

If the natural ramp compensation ($\delta_{natural\_comp}$) is higher than the ramp compensation needed ($\delta_{comp}$), the power supply does not need additional ramp compensation. If not, only the difference ($\delta_{comp}$–$\delta_{natural\_comp}$) should be used to calculate the accurate compensation value.

Thus the new division ratio is:

$$\text{if } \delta_{natural\_comp} < \delta_{comp} \Rightarrow \text{Ratio} = \frac{S_{sense}(\delta_{comp} - \delta_{natural\_comp})}{S_{int}} \quad \text{(eq. 52)}$$

Then $R_{comp}$ can be calculated with the same equation used when the natural ramp is neglected.

If we assume that our forward is based on the following information:

2 switch−Forward Power supply specification:

- Regulated output: 12 V
- $L_{out}$ = 27 μH
- $V_f$ = 0.5 V (drop voltage on the regulated output)
- Current sense resistor : 0.75 Ω
- Switching frequency : 125 kHz
- $V_{bulk}$ = 350 V, minimum input voltage at which the power supply works.
- Duty cycle max : $DC_{max}$ = 50%
- $V_{ramp}$ = 3.5 V, Internal ramp level.
- $R_{ramp}$ = 26.5 kΩ, Internal pull−up resistance
- Targeted ramp compensation level: 100%
- Transformer specification:
  - $L_{mag}$ = 13 mH
  - $N_s/N_p$ = 0.087

Internal ramp compensation level

$$S_{int} = \frac{V_{ramp}}{DC_{max}}F_{sw} \Rightarrow S_{int} = \frac{3.5}{0.50}125\text{ kHz} = 875\text{ mV/}\mu\text{s} \quad \text{(eq. 53)}$$

Secondary−side downslope projected over the sense resistor is:

$$S_{sense} = \frac{(V_{out} + V_f)}{L_{out}}\frac{N_S}{N_P}R_{sense} \Rightarrow S_{sense}\frac{(12 + 0.5)}{27 \cdot 10^{-6}}0.087 \times 0.75 = 30.21\text{ mV/}\mu\text{s} \quad \text{(eq. 54)}$$

Natural primary ramp:

$$S_{natural} = \frac{V_{bulk}}{L_{mag}}R_{sense} \Rightarrow S_{natural} = \frac{350}{13 \cdot 10^{-3}}0.75 = 20.19\text{ mV/}\mu\text{s} \quad \text{(eq. 55)}$$

Thus the natural ramp compensation is:

$$\delta_{natural\_comp} = \frac{S_{natural}}{S_{sense}} \Rightarrow \delta_{natural\_comp} = \frac{20.19}{30.21} = 66.8\% \quad \text{(eq. 56)}$$

Here the natural ramp compensation is lower than the desired ramp compensation, so an external compensation should be added to prevent sub−harmonics oscillation.

$$\text{Ratio} = \frac{S_{sense}(\delta_{comp} - \delta_{natural\_comp})}{S_{int}} \Rightarrow \text{Ratio} = \frac{30.21(1.00 - 0.67)}{875} = 0.0114 \quad \text{(eq. 57)}$$

We can know calculate external resistor ($R_{comp}$) to reach the correct compensation level.

$$R_{comp} = R_{ramp}\frac{\text{Ratio}}{1 - \text{Ratio}} \Rightarrow R_{comp} = 26.5 \cdot 10^3\frac{0.0114}{1 - 0.0114} = 305\ \Omega \quad \text{(eq. 58)}$$

Thus with $R_{comp}$ = 330 Ω, 100% compensation ramp is applied on the CS pin.

As the ramp compensation resistor is now calculated, we are able to calculate the capacitor value of the RC network connected to the CS pin.

If we assume the time constant of the RC network is equal to 220 ns, the capacitor value will be:

$$C_{CS} = \frac{\tau_{RC}}{R_{Comp}} = \frac{220\ n}{330} = 666\ pF \qquad \text{(eq. 59)}$$

If we select a 680−pF normalized value for $C_{CS}$ we are really close to the targeted time constant of 220 ns.

The following figure illustrates the behavior of the RC filtering network.

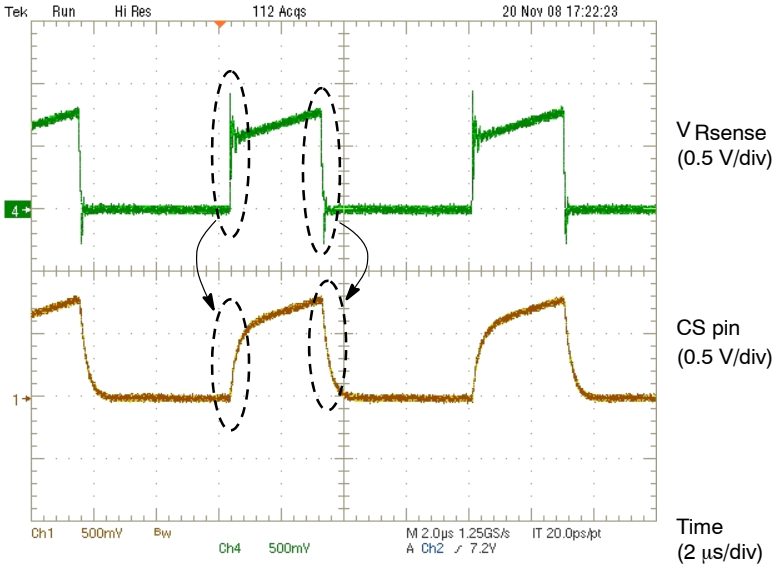


**Figure 15. Comparison of the Voltage on the Current Sense Resistor and After the RC Filter**

After filtering the current information of the forward converter provided to the controller is free of noise.

Note: The measurements done in Figure 15 have to be done by respecting a true clean ground probe connection. Usually the scope probe is delivered with a long ground wire: if the original ground wire is used, the current measurement will be worse than in reality. The following figure shows a comparison of the wrong and correct current measurements over the sense resistor.

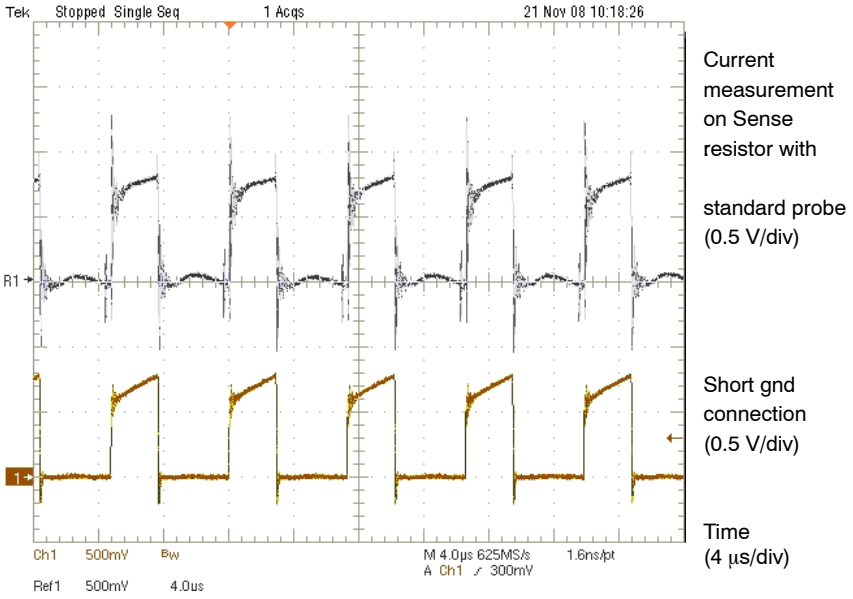


**Figure 16. Current Sense Measurement on Sense Resistor with Standard and Short Ground Connection**

Both following figures illustrate the different probe connection for measuring the current sense information.

Figure 17 illustrates the standard probe connection: but as the probe's ground wire is quite long, the measurement generates noise (see Figure 16 probe measurement comparison).

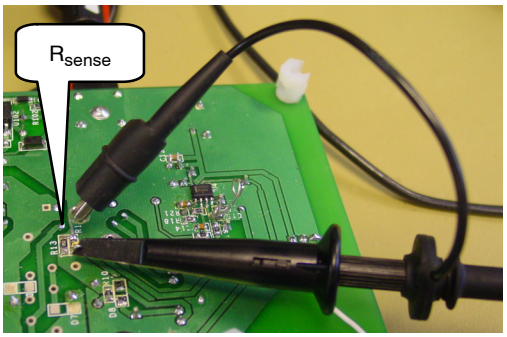


**Figure 17. Current Sense Measurement on Sense Resistor with Standard Probe Connection**

Figure 18 illustrates the correct connection for measuring on a power supply the current sense information. This connection has been done just by removing the plastic tips protection of the standard probe and by soldering two short wires directly to the sense resistor pads.

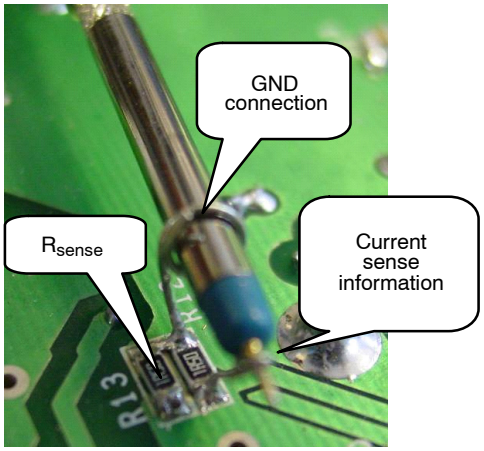


**Figure 18. Current Sense Measurement on Sense Resistor with Short Ground Connection of the Probe**

**Secondary diode snubber calculation:**

Without snubbing elements (R2&C2, R4&C6) in parallel with the secondary diodes (D5): some oscillations appear across the secondary diode. These oscillations are the result of the leakage inductance of the secondary side of the transformer with the capacitor behavior of the diode when it blocks. Thus in the worst case condition (max input voltage) it is possible that the maximum reverse voltage of the diode has been reached; with all the consequence.

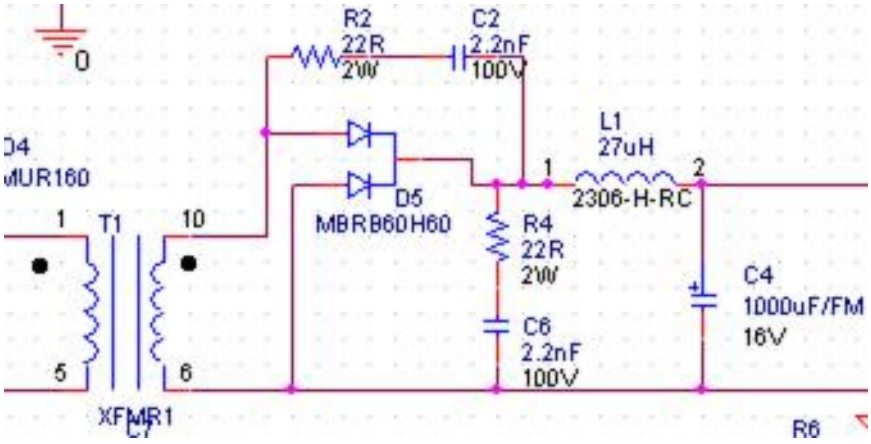


**Figure 19. Secondary Diode Snubbing**

As depicted by the following figure without snubbing element the oscillations at the nominal input voltage reach the maximum reverse voltage of the diode (60 V).

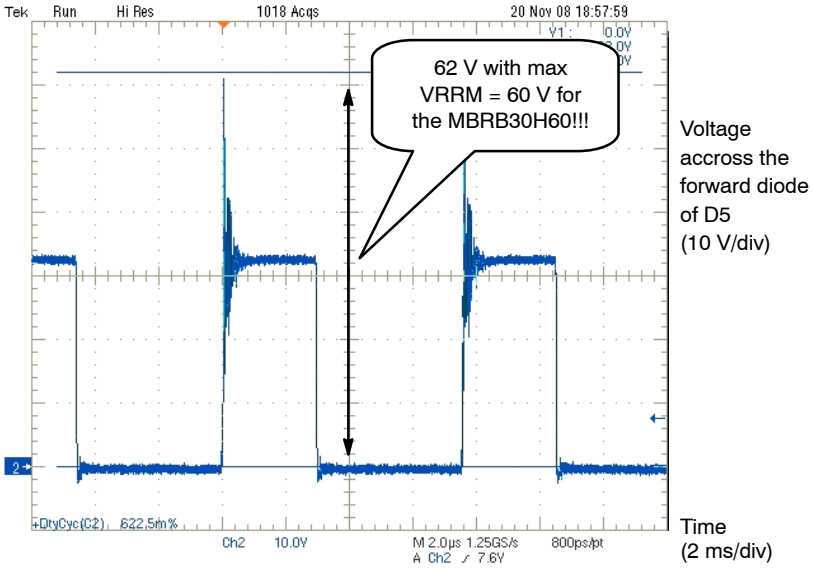


**Figure 20. Voltage Applied to the Forward Diode of D5**

The principle of the snubber placed in parallel of each diode is damp the oscillations. The oscillations take place at the end of the conduction of the diode and they are the consequences of the leakage inductance of the secondary winding and the parasitic diode behavior of the diode.

Knowing the leakage inductance of the secondary winding of the transformer and the oscillation frequency we are able to determine the resistor to be placed in parallel of the diode to damp the oscillations. In that case the resistor will be adjusted to damp completely all the oscillations implying a quality coefficient (Q) of 1:

$$R_{damp} = L_{leak}\omega_r = 118\ n \times 2\pi \times 22\ M = 16\ \Omega \quad \text{(eq. 60)}$$

After selecting a 22−Ω resistor for both secondary diodes, the oscillation voltage is now limited to 36 V compared to 62 V without snubber at similar input voltage (373 Vdc). A 2.2−nF capacitor is placed in series with the resistor in order to limit the losses due to the resistor presence.

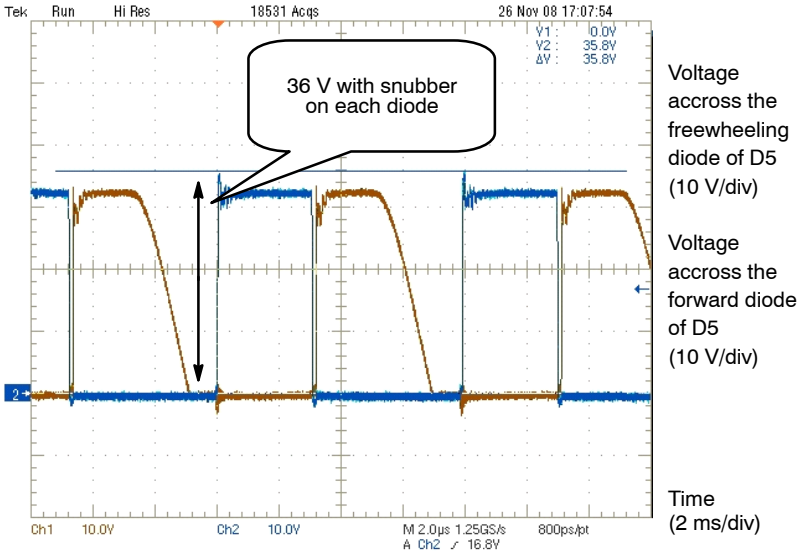


**Figure 21. Voltage Applied to the Secondary Diodes (D5) with Snubber**

## Board Performances

The following figures illustrate the general performances of this demoboard.

### Startup Delay

As depicted by Figure 22, when the $V_{CC}$ voltage is rising from zero and crossing $V_{CC(ON)}$ level, the NCP1252 sends the first pulses on the DRV pin only when the 120−ms startup delay is elapsed.

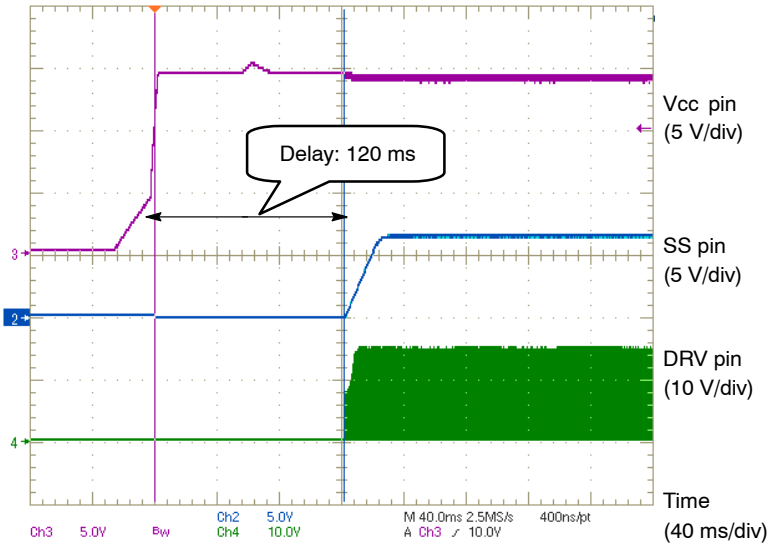


**Figure 22. Startup Delay**

### Soft Start

Figure 23 depicts a soft start sequence. The CS pin voltage is following the shape of the SS pin voltage. At the beginning of the soft start period, the peak current variation is not linear compare to the middle and the end of the soft start: this non linearity is related due to the DCM (Discontinuous Current Mode) mode of operation of the forward during the first 2 or 3 ms of the soft start when the output voltage is low (< 1 V).

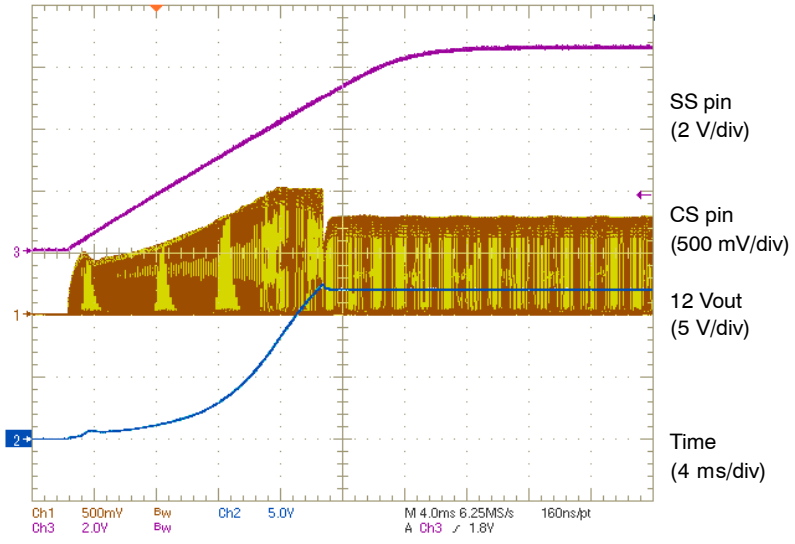


**Figure 23. Soft Start at Full Load (10 A)**

### Jittering Frequency

The Jittering frequency featured by the NCP1252 helps to spread out the switching noise and eases the filtering of the power supply. The following figure illustrates the digital jittering frequency of the NCP1252: ±5% of the centered switching frequency selected by the resistor connected to $R_t$ pin with a frequency modulation of 330 Hz. The jittering modulation can be also observed by measuring the $R_t$ pin voltage.

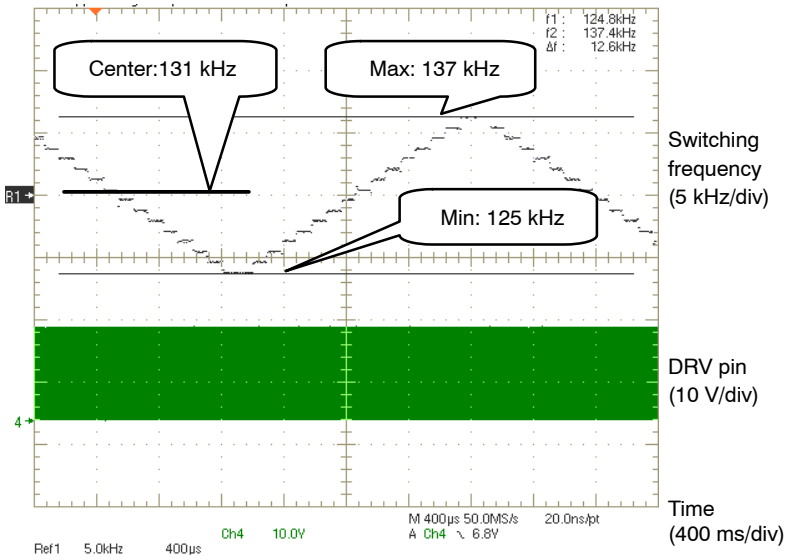


**Figure 24. Jittering Frequency Measurement**

### No Load Regulation

Thanks to the skip cycle feature implemented on the NCP1252, it is possible to achieve a real no load regulation without triggering any over voltage protection. The demonstration board does not have any dummy load and ensure a correct no load regulation. This regulation is achieved by skipping some driving cycles and by forcing the NCP1252 in burst mode of operation.

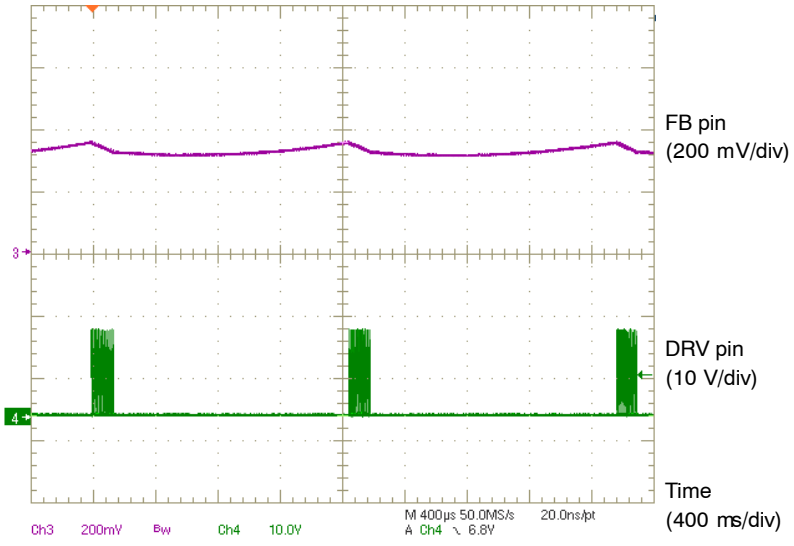


**Figure 25. No Load Regulation (Real No Load to the Output) Vout = 12.096 V**

### Step Load Stability

In order to test the close loop stability, a maximum step load of 5 A have been applied on the output. The following figures show the fast transient response without any oscillations and exhibit a low drop voltage 165 mV (1.3% of the nominal output).

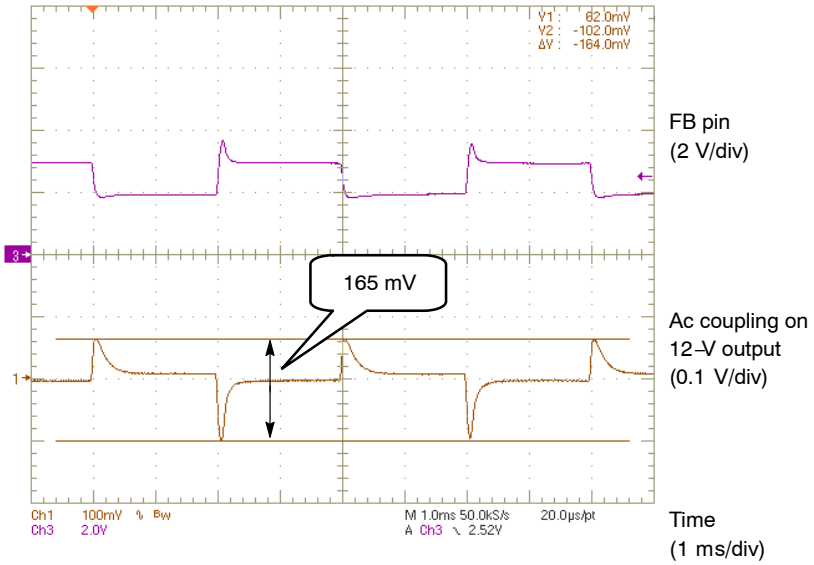


**Figure 26. Step Load Response from 5 A to 10 A**

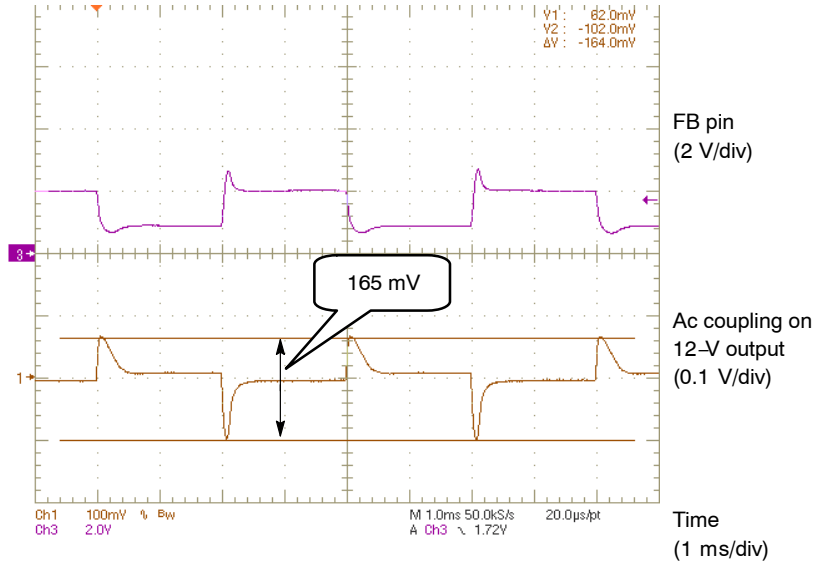


**Figure 27. Step Load Response from 0.5 A to 5.5 A**

**Efficiency**

The efficiency measurements have been done at room temp at different load conditions and at the nominal load with different input voltage.

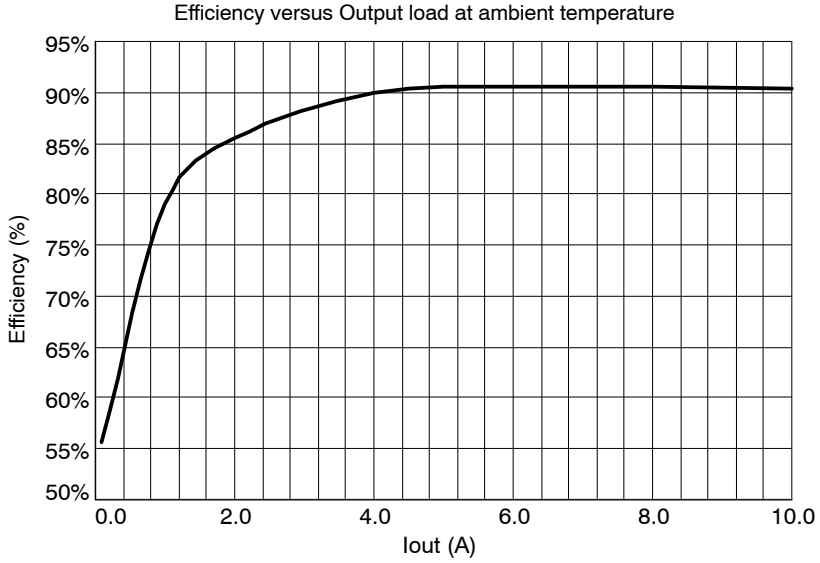


**Figure 28. Efficiency Measurement at Room Temperature and Nominal Input Voltage (390 V dc) versus Output Load Variation**

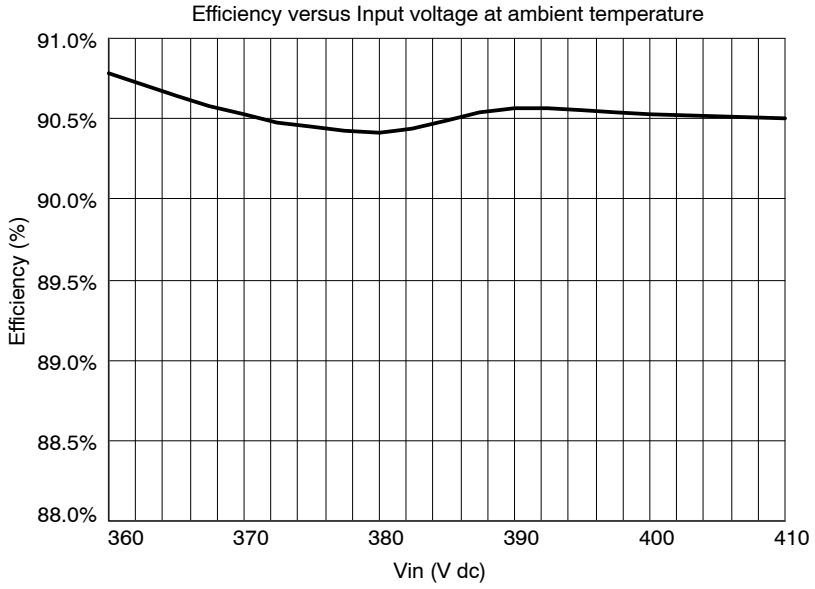


**Figure 29. Efficiency Measurement at Room Temperature and Nominal Output Load (10 A dc) versus Intput Voltage**

One possible way to improve the efficiency of the demoboard is to implement a synchronous rectification, it will improve by some percent the overall efficiency.

## Demoboard Schematics

### Main Board with its Auxiliary Supply

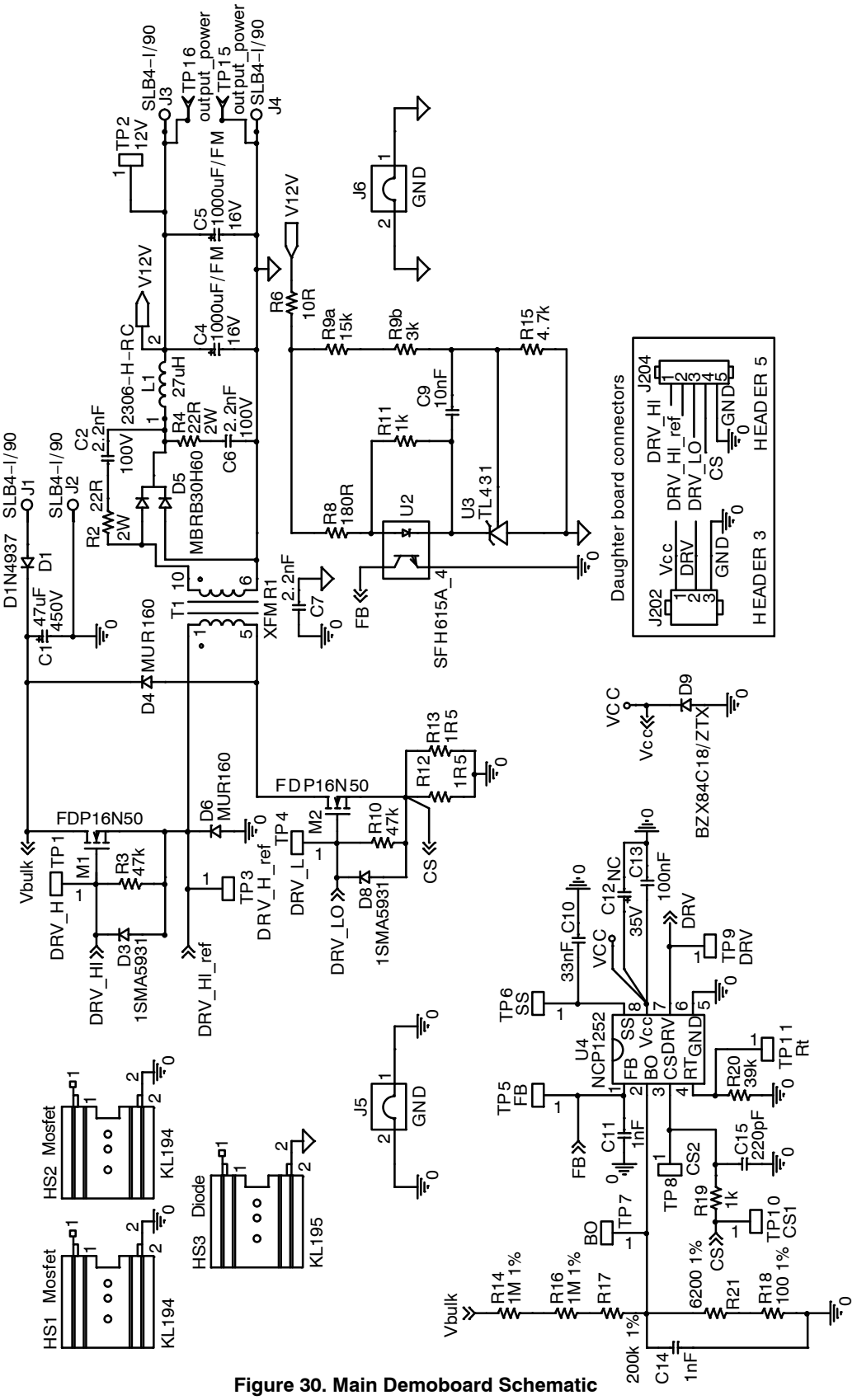


**Figure 30. Main Demoboard Schematic**

As depicted by Figure 30, the NCP1252 feedback is implemented via a TL431 arranged in a Type 2 corrector. The power supply can be connected directly to a dc source, where the minimum startup voltage is 370 Vdc. There are 2 options for supplying the Vcc to the NCP1252:

- External $V_{cc}$ supply: in that case the dedicated connector for the $V_{cc}$ can be used to supply the 15 Vdc to the demoboard. The NCP1010 controller for the auxiliairy supply must be removed from the board.
- Self $V_{cc}$ supply: in that case the NCP1010 regulator (see Figure 31) is used to build the 15 V output via a buck converter for stepping down the main bulk voltage to the $V_{cc}$ level. This auxiliary self supply is implemented on the main board close to the bulk voltage.

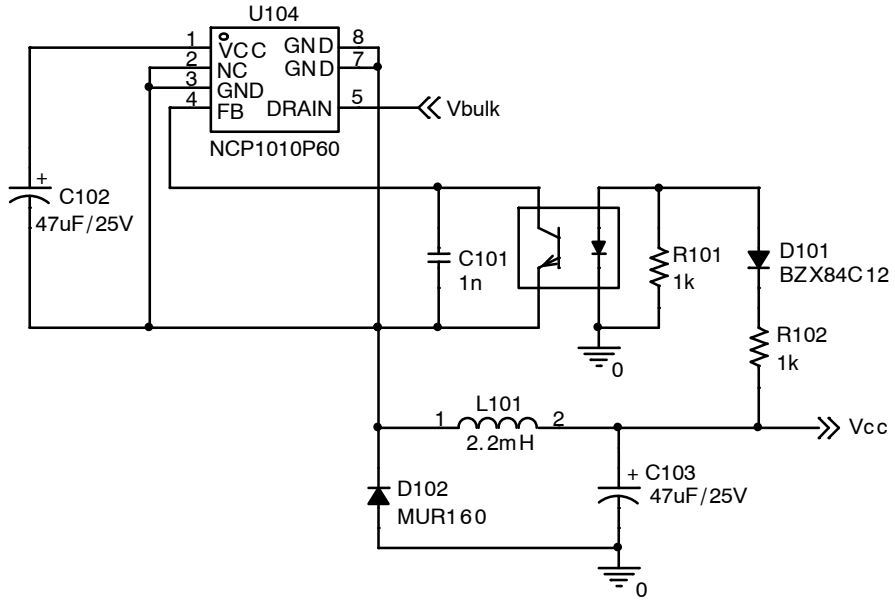


**Figure 31. Auxiliary Supply Based on the NCP1010 @ 65 kHz**

**Daughter Board: Driver Stage**

The daughter board or the drivers for the high side and low side mosfet is done with a pulse transformer from PREMO. We selected to drive also the low side power mosfet with the pulse transformer to prevent any difference on the way to drive the low and high side mosfet.

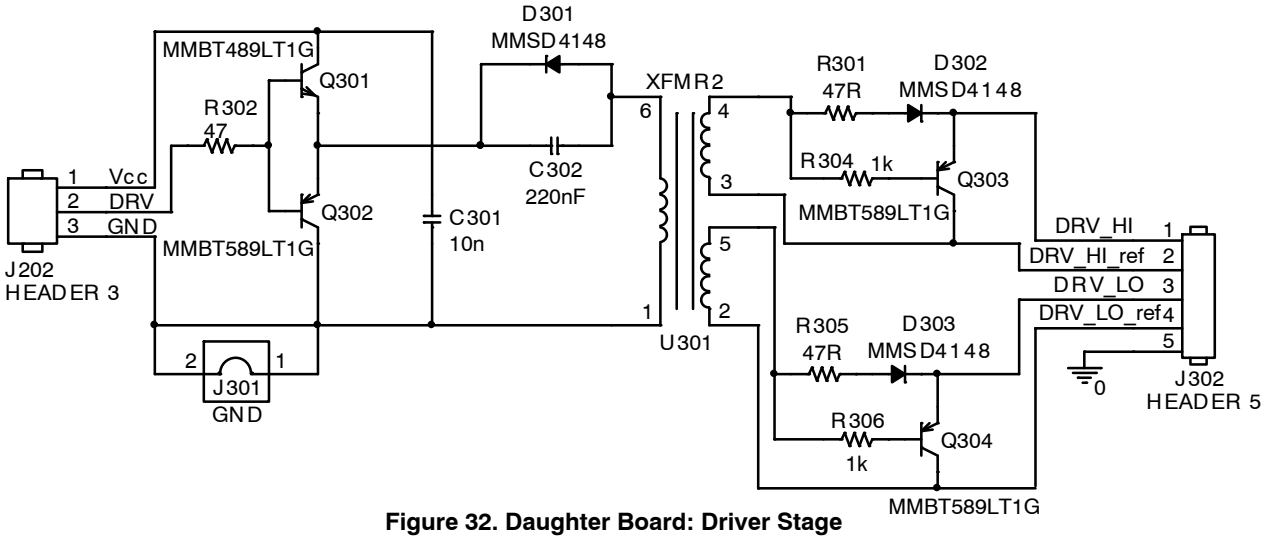


**Figure 32. Daughter Board: Driver Stage**

## Demo Board Picture

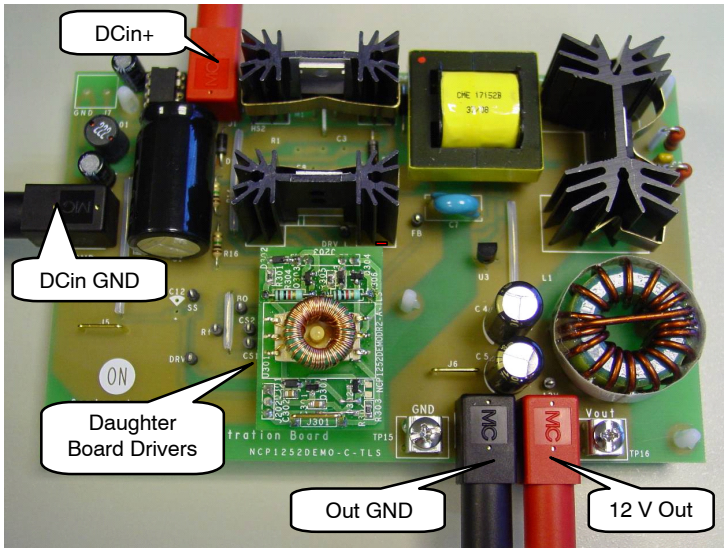


**Figure 33. Top View of the Demo Board**

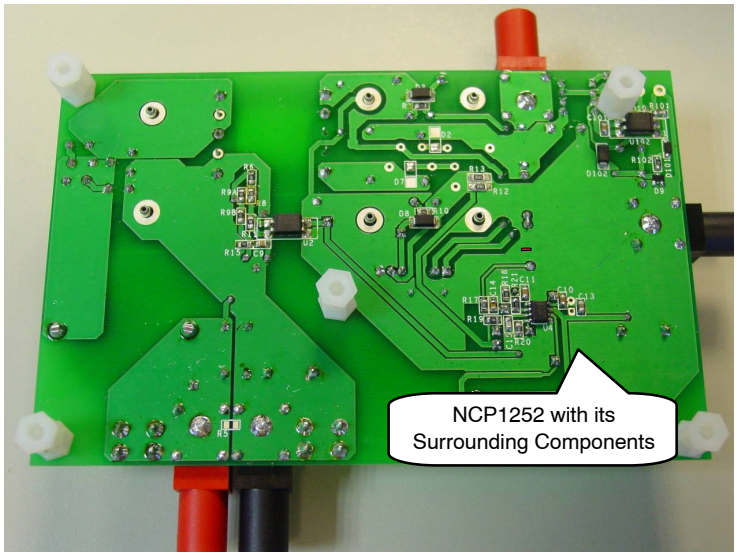


**Figure 34. Bottom View of the Demo Board**

## References

1. C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw−Hill, 2008.
2. Heatsink manufacturer link: http://www.seifert−electronic.de/en/produkt.php?id=50 or direct link to the datasheet http://www.digtion−medien.de/seifert/Uploads/seifert_punkte/pdfs/50%5B0%5D.pdf



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